

1Team[®]-System

Comprehensive Analysis of SystemC Code
for Early Design Closure



The quality of the original conceptual source for a design dictates the quality & speed of validation and implementation. SystemC provides expressive power for fast simulation, but needs validation and style constraint to be effective in an implemented system design flow. Atrenta's SystemC solution addresses these challenges with a broad based solution starting early in design process and validation throughout the SystemC design development.

The Problem

- SystemC allows high level modeling at higher speeds.
- Powerful in concept, it is unfamiliar to most designers, so achieving productive usage takes a steep learning curve.
- Incorrect SystemC may apparently simulate correctly.
- Typical SystemC tools use gcc front ends to compile SystemC, resulting in class-based error messages which do not communicate the error to most designers.
- Most SystemC tools expect a specific style, version and subset of SystemC – whereas a flow needs one source compatible with all downstream tools.

The 1Team-System Solution Supports All SystemC Elements

Methodology-Specific Libraries Master/Slave Library, etc.	Layered Libraries Verification Library TLM Library, etc.
Primitive Channels Signal, Fifo, Mutex, Semaphore, etc.	
Structural Elements Modules Ports Interfaces Channels	Data Types 4-valued Logic Bits and Bit Vectors Arbitrary Precision Integers Fixed-point Types
Event-driven Simulation Events Processes	
C++ Language Standard	

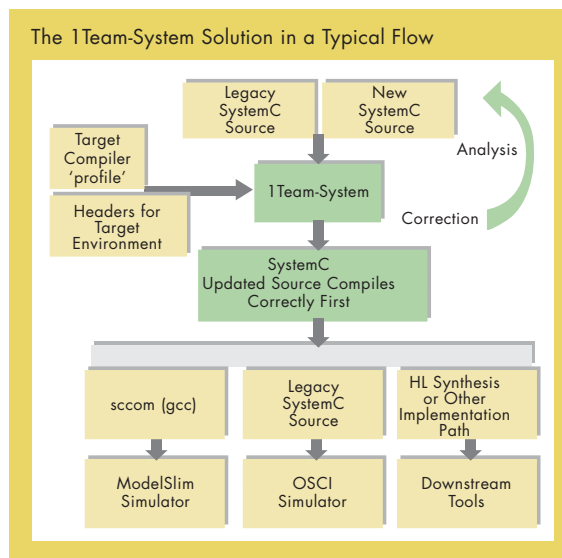
Source: systemc.org

Existing Solutions

- Simulation tools focus on the design function with user-supplied vectors.
 - > First you have to compile your SystemC then link to the simulation kernel. Unfortunately typical compile-and-link tools are neither design nor simulation oriented.
 - > To achieve performance, SystemC simulation is simplified. Simulators may not catch design structure errors e.g. connected outputs.
- Manual design reviews help, but the process is tedious and error-prone.
 - > Acceptable simulation style may not be ideal for synthesis or other downstream tools.

The Atrenta Solution – 1Team-System

- Based on industry standard SpyGlass technology.
- Analyzes and optimizes SystemC code for correctness and consistency.
- Supports SystemC 2.0.1, 2.1, IEEE1666 (2.2) & 2.0.1→2.1, 2.1→IEEE 1666 (2.2) migration checks.
- Analyzes mixed C++/SystemC code from TLM to RTL.
- Enforces compliance with corporate and industry standards.
- Configurable best practices: captures and automates system-level coding expertise.
- Integrated debug environments speed analysis and source code debug/edit.
- Real-time feedback on SystemC coding hazards for structure, simulation and synthesis.



The Atrenta Difference

- Enables fast time-to-expertise and fast time-to-diagnosis for non-experts.
- Reduces implementation costs by ensuring SystemC code meets system-level objectives.
- Accelerates SystemC adoption and path to expertise.
- Facilitates scalability of SystemC expertise to speed team deployment.
- Quickly isolates root causes, preventing cascading error messages.
- Reduces iterations and debug-time during simulation and synthesis of SystemC code.
- Facilitates IP reuse by enforcing corporate standards and best practices.
- Easy to ramp up and begin productive use within half a day.

Available now on Unix and Windows platforms, and is integrated in industry standard IDEs



CONTACT:
1.408.453.3333
moreinfo@atrenta.com
www.atrenta.com

Atrenta Inc. is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools & methodologies to capture design intent, explore implementation alternatives, validate RTL and optimize designs early, before expensive and time consuming detailed implementation. With over 140 customers, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. **Atrenta, Right from the Start!**

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