

1Team[®]-Genesis Physical

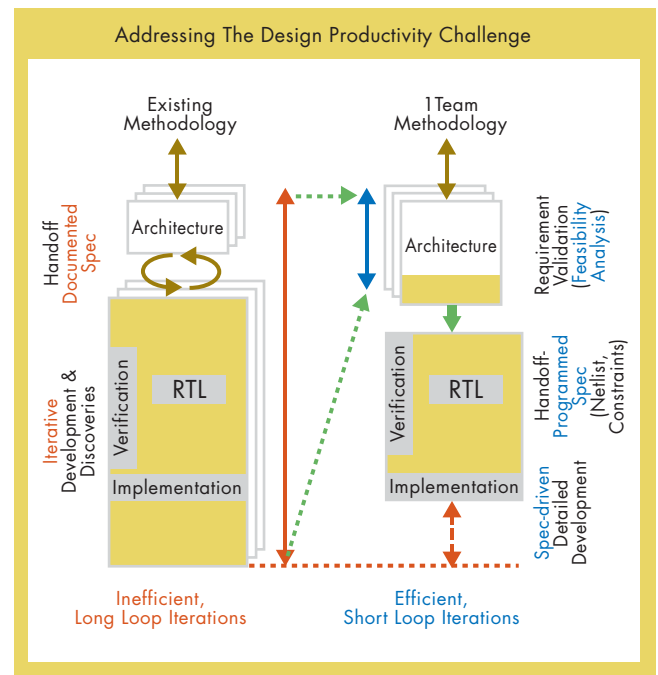
Early Physical Feasibility Analysis



Design closure at RTL is the much-awaited evolution in the industry. It provides a clean hand-off, it satisfies the ever-increasing need for designers to make important trade-offs early in the design process and leverages the significant impact RTL changes have on timing and physical feasibility. Present solutions strive for physical and timing closure at the gate level with challenging iterations between back-end and front-end design, which span different design teams. Atrenta's 1Team-Genesis Physical solution provides a true RTL prototyping environment that helps SoC Architects and RTL designers analyze, visualize and modify the design to achieve physical and timing closure at RTL.

The Problem

- SoC Architects need to know the timing and physical feasibility of the design at the early-RTL stage, in order to manage the design project and make important trade-offs to achieve design goals
- RTL designers need to know the physical congestion and timing challenges of the RTL code to make high impact changes early in the design flow
- Design closure at later stages of the design (at the gate-level) is often difficult and sometimes impossible - changes that can be effectively made at this stage of the design do not have the necessary impact to attain the desired goal
- Debugging the design at the gate-level versus driving the solution from RTL, burdens both front-end and back-end teams
- RTL source designers have to wait for iterative feedback from back-end teams for assessment of physical and timing closure - this feedback is of limited value as it does not tie back to the RTL source

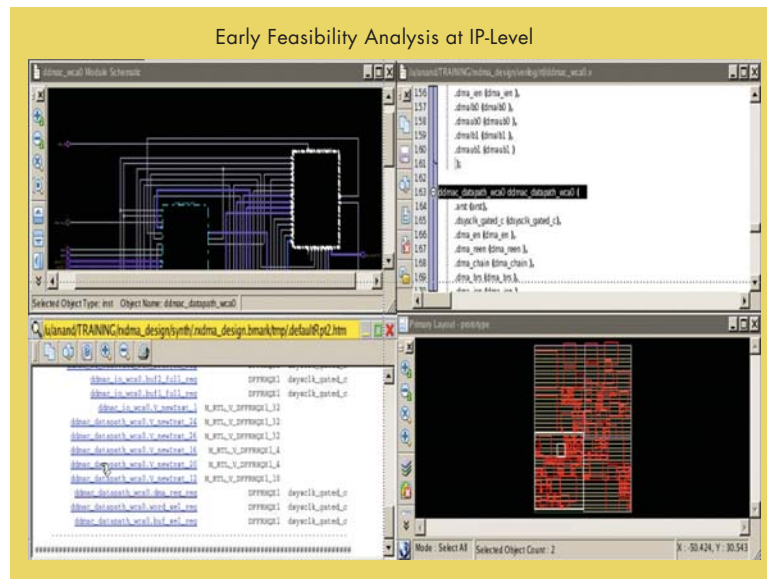


Existing Solutions

- All physical (congestion) and timing analysis is available today only at the gate-level back end
- A successful solution with gate level timing closure involves several long iterations from the gate level back-end to the RTL front-end - problems are identified late in the back-end and communicated back to the RTL front end
- Prior RTL prototyping solutions lacked the robust mix and integration of technologies (synthesis / STA /automatic floorplanning /congestion analysis) with appropriate consideration for performance/ capacity/accuracy. They also lacked a reliable tie back to the RTL source
- At best, RTL designers obtain some visibility into performance and area based on inaccurate wireload model-based synthesis
- Design closure requires generation of floorplans - presently, generating floorplans for SoC designs with hundreds of hard macro blocks is a difficult manual effort
- RTL designers usually do not have physical expertise; Physical designers do not have insight or ability to change RTL - design closure relies on challenging cross-team interactions

The Atrenta Solution – 1Team®-Genesis Physical

- Captures a working specification of the design in the early phase which evolves with the project
- Provides early analysis, prediction and visualization of timing, area and congestion for architects and RTL designers
- Aids SoC architects to make critical architectural trade-offs early in the design phase: such as the choice of slow vs. fast memory; 130 vs 90 nm process; choice of design partitions
- Enables RTL designers to make high impact micro-architectural changes to achieve physical & timing goals of the design
- Accelerates floorplanning of large and complex designs - floor plans provide a vital seed for physical designers



- Empowers designers to select the best of alternate floorplans to hand-off to backend tools
- Delivers physical & timing closure to designers at RTL

The Atrenta Difference

- A true RTL prototyping environment that preserves RTL constructs and ties the logical, physical and timing domains to the RTL source -this enables accurate analysis and design closure at RTL
- Intuitive GUI environment with all-way cross-probing to RTL from schematic, logical hierarchy, physical and timing views. Offers easy visualization of the RTL's impact on design goals
- Robust technology infrastructure (synthesis/STA/automatic floorplanning/congestion analysis) that enables fast, high capacity and accurate RTL prototyping for quick trade-offs and rapid design closure
- Hands-free physical - SoC architects and RTL designers analyze and modify their design for physical and timing closure – without requiring physical expertise
- Various hand-offs - RTL, netlist, or floorplan to downstream implementation tools – all of which fit easily with existing design flows
- Reduced TAT - elimination of long, tedious iterations from gate level back-end to front-end for design closure
- Predictable TAT - early ability to analyze and modify design feasibility (at RTL) versus respond to late discoveries (at the gate level) yields manageable and predictable design schedule



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Atrenta is the leading provider of Early Design Closure® solutions that radically improve the efficiency of integrated circuit design. Using Atrenta's comprehensive tool suite for architectural chip assembly and RTL analysis, customers can create robust and correct designs rapidly, preventing expensive and tedious iterations during the implementation phase. With over 150 customers worldwide, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. Atrenta, Right from the Start!