

1Team[®]-Genesis Registers

Automated Register Management



With an increase in design complexity coupled with time-to-market pressures, semiconductor product development companies have started to focus on IP reuse and platform-based design techniques with renewed vigor. One major challenge in integrating IPs from multiple vendors in platform-based designs is managing the vast number of registers, which are typically part of all complex designs and reside across multiple IPs. The 1Team[®]-Genesis Registers solution simplifies the highly arduous process of manually managing the registers of an SoC and creating the relevant memory maps. This enables the design, verification and software teams to work more efficiently from consistent and synchronized views of the chip design.

The Problem

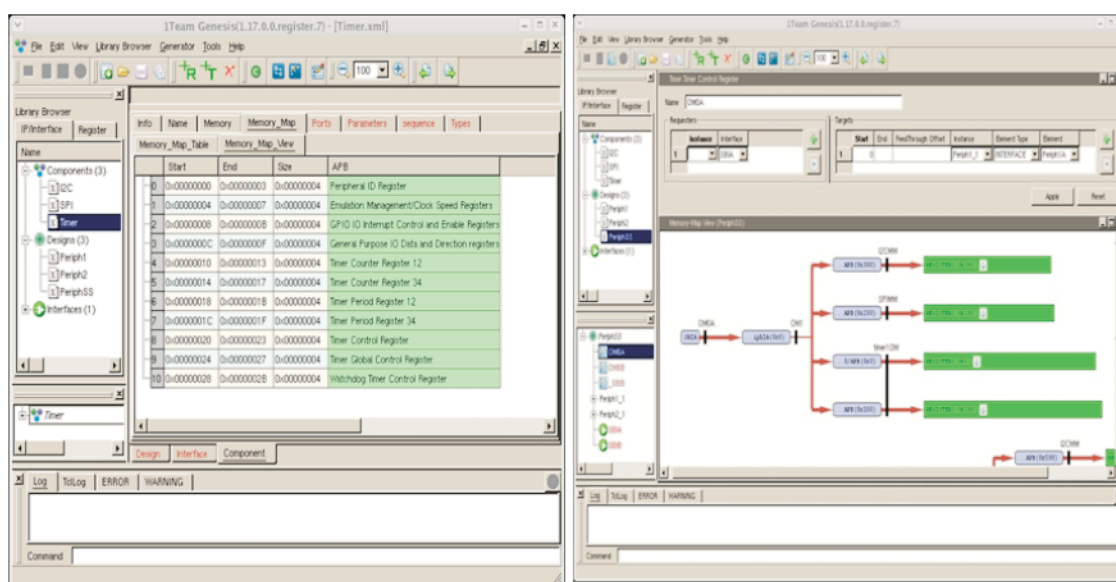
The process of manually managing the definitions and usage of on-chip registers that are part of a complex SoC across different design and software teams is very often laborious and inefficient. Each team has its own conceptual view, usage model and preferred style for documentation and this inevitably creates considerable confusion on various fronts such as interpretation of register definitions, bit assignments, etc., causing undesirable delays during product development. Hence the need for the different teams to work more efficiently from consistent and synchronized views of the register and memory maps. Further, as design teams become geographically dispersed, consistency and correctness of design implementation data becomes a key challenge for software development and chip integration teams.

The Atrenta Solution – 1Team-Genesis Registers

- Centralized repository for all register and memory map definitions and use models for all IPs, sub-systems or SoCs
- Provides unique value to different cross-functional teams, while maintaining a consistent and synchronized view of the design
 - SoC/IP designers: Provides detailed definition and usage information of the registers for design implementation
 - Software designers: Provides global view of the sub-system through the registers enabling earlier software integration. Generates C/C++ header files for components and design address maps
 - Verification designers: Provides consistent usage information for generating the test vectors for hardware/software co-simulation. Minimizes scope of data misinterpretation between the various design teams
 - Documentation team: Automates the creation of user manuals for different customers
- Comprehensive register modeling with support for parameterization, conditional registers, alternative bit fields, modes, dependency, etc.

The Atrenta Solution – 1Team-Genesis Registers (Contd.)

- Automatic generation of hierarchical address maps. Provides component and sub-system address maps, mode address maps (e.g., boot-mode, kernel-mode) and displays registers mapping for each requestor
- Completely customizable generators:
 - Templates
 - C/C++ header files for components and design address maps
 - RTL model of registers for verification/software co-simulation
- Provides documentation about usage models for downstream users such as RTL designers, verification engineers and end users in styles that is relevant to them (e, HTML, WordML, etc.)
- Development kits for customization – Provides support for Perl Template Toolkit (PTT), style sheets and structured documents
- Flexibility in defining registers using spread sheets, GUI or Tcl
- On the fly checks for data coherency
- IP-XACT support



The Atrenta Difference

- Addresses all elements of register management, including description and generation of control register logic, assertions and verification models, software interfaces, and the accurate documentation necessary for system-level design
- Helps dispersed design teams to create more consistent, high-quality designs
- Tight integration with the Genesis-Assembly provides a complete hardware/software interface solution that accelerates IP integration and design re-use
- Integrates seamlessly into existing design environments, dramatically enhancing efficiency of installed tools and methodologies



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