

SpyGlass®-Constraints

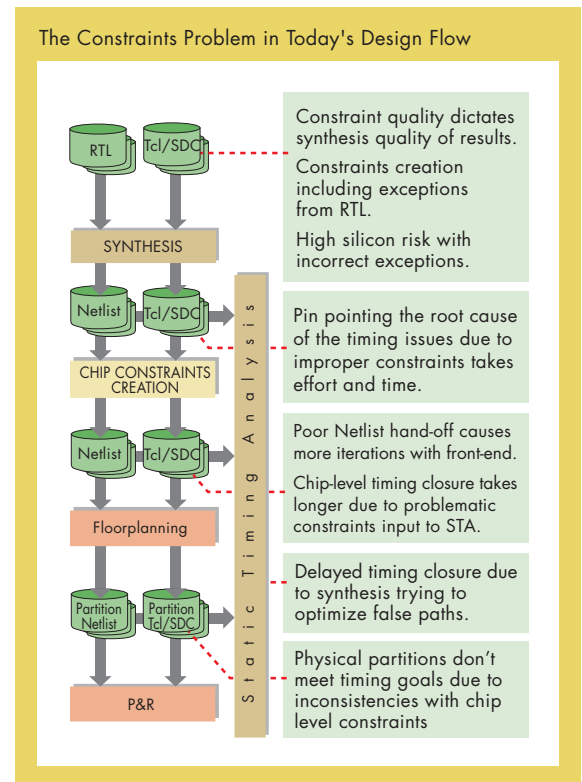
Specify Early, Validate Continuously
& Automate Handoff



Quality of constraints dictates the quality and speed of implementation. Constraints impact is multi-dimensional spanning synthesis, timing analysis, and physical design. More than 25% of design projects go through more than 10 iterations due to constraints issues. The burden of overall constraints effectiveness is on the design engineers across the development process. Atrenta's SpyGlass®-Constraints solution addresses these challenges with a broad based solution starting early in design process and providing an environment to validate continuously.

The Problem

- Must avoid silicon re-spins:
 - > Incorrect timing exceptions results in silicon failing timing
- Design schedules are not predictable:
 - > Creating/updating constraints is error prone; More Iterations result from changing constraints
- IP reuse has become critical:
 - > Poor constraints reduces IP reuse by 50%
- Time to market has become critical:
 - > Timing closure takes 50% more time with poor constraints
 - > Timing budgeters are not doing a good job of creating block constraints from the top level
- Existing solutions do not adequately address constraint problems:
 - > Simulation tools use test vectors designed for the design function, whereas, constraints are designed for timing. Logic equivalency checking tools verify the design function, not the constraints; static timing analysis produce bad timing given bad constraints

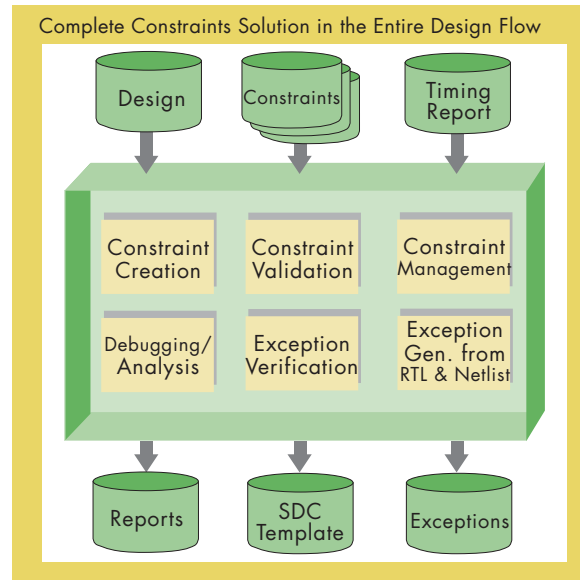


The Atrenta Solution – SpyGlass-Constraints

- Constraint Creation: Generates constraints template and exceptions from RTL or Netlist; facilitates error-free creation of constraints quickly that results in higher quality of results from implementation tools
- Constraint Management: Automates chip constraints creation by merging block constraints for faster chip level timing closure; reports equivalence in SDC versions at different stages of the design, resulting in reduced iterations
- Constraint Validation: Pinpoints syntax, consistency as methodology issues; covers intra-block, inter-block, blocks versus chip. Consistent constraints reduces iterations and speeds up implementation
- Exception Verification: Eliminates incorrect exceptions that can mask silicon timing failure. Reduces silicon timing risk
- Timing Critical Exception Generation: Creates exceptions among timing critical paths that improve implementation quality of results

SpyGlass-Constraints Methodology

- Provides a structured, easy to use and a comprehensive method for solving constraint problems that ensures quality results with fewer but meaningful violations, thus saving time
- Provides methodology documentation and rule-sets as part of the product
- Walks users through a series of recommended steps to optimize constraints at block level, as well as, chip level constraints at RTL, pre-layout and post-layout stages -the steps include design setup, creating new SDC components, cleaning clock and delay constraints, fixing timing exceptions, resolving hierarchical constraints, and creating timing-critical timing exceptions post-static timing analysis



The Atrenta Difference

- Complete solution:
 - > Supports native PrimeTime Tcl as well as SDC.
 - > Supports constraints checking, management, and creation based on both structural and formal techniques
 - > Supports timing criticality based false path identification which considers both function and timing aspects
 - > Integrates with Atrenta SpyGlass capabilities targeted for RTL like low power, clock domain crossing and DFT
- Superior solution:
 - > Provides highest completion rate, especially of sequential false path and MCP verification.
 - > Provides a robust combinational and sequential false path verification solution
 - > Provides best-in-class exception verification in terms of accuracy and runtime
- Best debug and analysis solution:
 - > Includes cross-probing to Tcl/SDC, schematic and design source
 - > Provides most comprehensive reporting of exception verification results
- Easy to deploy:
 - > Includes rulesets and tutorial enables quick adoption by engineers and constraints optimized design
 - > Complements, and plugs straight into, standard EDA flows



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Atrenta Inc. is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools & methodologies to optimize their designs early in the RTL phase for linting, clock domain crossings, power estimation and reduction, design for test, constraints generation and validation including timing exceptions, and RTL prototyping. **Atrenta, Right from the Start!**

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