

# SpyGlass®-DFT

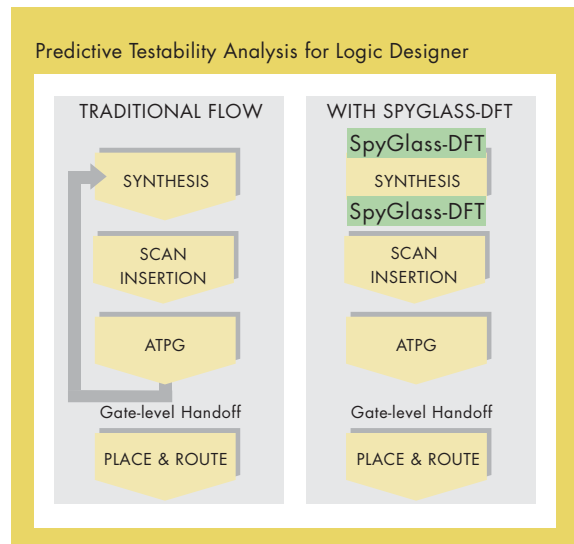
Design-for-Test at RTL and Achieve Early Design Closure®

THINK  
**EARLY  
DESIGN  
CLOSURE**  
THINK  
ATRENTA®

With the rapidly soaring cost of silicon especially at 130nm and below, testability of designs is becoming a key aspect of design closure. While there are tools that address test issues at gate-level, achieving high test coverage entails designing for test early in the design cycle. The SpyGlass®-DFT solution is the only tool that comprehensively enables early test closure at RTL. It has the unique ability to predict test coverage at RTL, pinpoint testability issues in the design and even fix those issues automatically. Geared for RTL designers, it removes the burden of fixing test or timing closure issues at later stages of design implementation.

## The Design-for-Test Problem

- Test coverage analysis is typically done at late stages of design implementation or sometimes even after silicon is out, leading to design iterations or worse even silicon re-spins.
- Designers cannot afford to have low test coverage, which directly correlates to test quality and thereby yield, especially with the rapidly increasing cost of silicon; most semiconductor vendors have made it mandatory now for achieving over 99% test coverage for stuck-at, and 80% for transition delay faults.



## The At-speed Testing Problem

- The test clocks in traditional stuck-at testing are designed to run on the test equipment at frequencies lower than the system speed. At-speed testing requires test clocks to be generated at the system speed, and these clocks are often shared with functional clocks from a phase locked loop (PLL) clock source. This additional test clocking circuitry affects functional clock skew, and thus the timing closure of the design.
- At-speed tests often result in lower than required fault coverage even with full-scan and high (>99%) stuck-at coverage. Identifying reasons for low at-speed coverage at ATPG stage is too late to make changes to the design and affects schedules significantly.

## The Atrenta Solution – SpyGlass-DFT

- Ensures RTL is scan-compliant and yields high test coverage
- Pinpoints and diagnoses DFT issues starting at RTL
- Predicts ATPG test coverage with high correlation (within 1-2% of ATPG results)
- Identifies causes of low test coverage for stuck-at and transition delay faults at RTL, and helps achieve quick turnaround times for today's aggressive design schedules and time-to-market challenges
- Addresses the timing closure issues on functional clocks due to at-speed DFT
- Unique AutoFix capability automatically corrects RTL to improve scanability
- Built-in controllability and observability engine analyzes testability strategies
- Guides selection of highest-value test points
- SoC rules validate connectivity and integration at chip-level in the presence of different testmode constraints
- Intuitive, integrated debug environment with cross-probing among views

## SpyGlass-DFT Methodology

- Provides easy-to-use and a comprehensive method for solving Design-for-Test problems at RTL to ensure higher test quality
- Provides methodology documentation and rule-sets are provided as part of the product
- Results in fewer but meaningful violations, thus saving time for the RTL designer
- Walks users through a series of recommended steps to analyze DFT violations at block and chip level - the steps include design setup, defining initial test signals, scan wrapping black boxes, using by-pass constraints for modules with internal by-pass logic, achieving scanability, making latches transparent, adding test points, and validating scan chains

## The Atrenta Difference

- Integrates with Atrenta SpyGlass capabilities targeted for RTL like power, CDC and constraints
  - > Easy to ramp up and begin productive use within half a day, even for non-experts
  - > A structured methodology enables quick adoption by engineers and constraints optimized designs
- Enables RTL designers to design for test without having to become test experts
- Addresses testability in hours during RTL design— instead of spending days later in the cycle
- Estimates test coverage at RTL and help achieve high test coverage (98-99%) in golden RTL
- Removes tedious and error-prone manual fixes to RTL to fix testability violations with the AutoFix capability
- Ensures correct SoC integration for diverse testability strategies



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Atrenta Inc. is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools & methodologies to optimize their designs early in the RTL phase for linting, clock domain crossings, power estimation and reduction, design for test, constraints generation and validation including timing exceptions, and RTL prototyping. **Atrenta, Right from the Start!**

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