

SpyGlass®-MBIST

Vendor Independent RTL MBIST Solution



With the rapidly soaring cost of silicon, especially at 90nm and below, testability of memories is becoming a key aspect of design closure. Current designs have hundreds of memories which require built-in self test (MBIST) and repair logic insertion. It is desirable to validate the design with test logic inserted early in the design stage, as well as take the additional BIST logic area into consideration for design implementation and optimization. While there are tools that address memory test insertion and validation at the gate-level, better results can be achieved by inserting BIST and validating early in the design cycle, preferably at RTL, to achieve predictability and improve productivity. The SpyGlass®-MBIST product has the unique ability to insert MBIST at RTL with any ASIC vendor's qualified library and validate the new connections. Geared for RTL designers, it removes the burden of validating and fixing memory test issues at later stages of design implementation.

The Problem

Advanced designs have hundreds, if not thousands of memories. It is imperative to test all the memories in the design by inserting memory built-in self test along with repair logic to gain high yields.

Traditionally, designers synthesize the design first to a gate level representation and then hand it over to the ASIC vendor to insert MBIST logic at the netlist level.

When MBIST is inserted at the gate level:

- Functional verification takes longer and is expensive and is not in control of the system house/designer
- Optimization during synthesis/early floor-planning does not take MBIST logic into account

- BIST sharing schemes and architectural trade-offs could result in many design iterations through RTL synthesis and floor-planning
- RTL for the design does not remain golden for IP handoff/reuse

There are also many tools on the market which are tailored to insert proprietary BIST architectures and libraries and work mainly at the gate level.

However, ASIC vendors and system houses need an RTL solution that is flexible and compatible with any vendor's BIST IPs, and provides automation for BIST insertion at RTL for faster design validation.

The Atrenta Solution - SpyGlass-MBIST

- Tightly integrates into the SpyGlass-DFT environment and ensures correct BIST insertion at RTL
- Validates new connections and makes sure that the design is scan-compliant and yields high test coverage
- Provides an automated process for capturing design-dependent and IP-dependent information
- Allows execution of the connections with support of global commands for definition of busses and/or repetitive wire-up through the hierarchy
- Allows multiple insertion capabilities and supports various BIST architectures and fuse-wrapper IP's;
- Inserts or replaces blocks in the design and inserts glue logic at the top-level
- Supports a bottom-up methodology for a hierarchical approach
- Provides timing constraints (SDC) promotion for synthesis and test insertion
- Allows a "dummy design" capability to preserve RTL confidentiality when the customer wants to hand over the netlist with BIST for validation at the ASIC vendor's site

SpyGlass-MBIST Mechanism

The SpyGlass-MBIST solution uses a multi-pass approach to prepare for the insertion of the BIST components and generate the modified RTL.

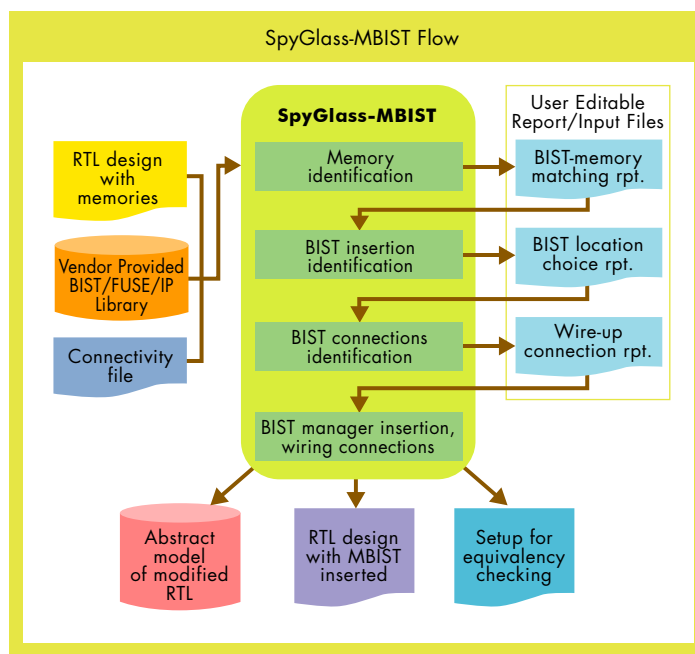
At the first stage, the memories are identified and the tool tries to match every memory to one or more appropriate BIST IPs available in the library supplied by the memory vendor. The designer then reviews the matching report and provides unique matching information.

At the second stage, the tool looks for the best insertion point of the BIST controllers and fuse controllers. The designer interacts and provides guidance about the desired insertion for the location of these new blocks.

Effort in the third stage is focused on establishing connections of the various BIST components with the BIST manager. Once again, the designer has the opportunity to review the connections and define specifications if required. Automated checks at this stage prevent the attempt of any illegal connections.

Finally, at the fourth stage, the tool produces the desired modified RTL. The output generated by the tool consists of the following:

- Desired modified RTL (used for synthesis and other downstream activities)



- Abstract model of the modified design (used for SoC integration and BIST insertion at the top level)
- Skeleton design with only the BIST logic and no functional RTL. This is usually supplied to the ASIC vendor to enable them to do any groundwork before the final physical implementation of the chip
- Necessary setup files (in a generic format) to work with a formal equivalence checker of the designer's choice

The Atrenta Difference - SpyGlass-MBIST

The benefits of RTL MBIST insertion are:

- Allows earlier and faster validation than at gate level as simulations are run at RTL
- Allows timing optimization of the complete RTL with BIST logic during synthesis
- MBIST area impact is known early
- DFT rules can be run at RTL that include MBIST logic

MBIST insertion/validation automation allows:

- BIST insertion to be transparent to the user like scan insertion
- Less errors compared to manual approaches resulting in improvement in design integration quality
- Predictability, providing reproducible results to control the design schedule
- Easy exploration of different MBIST strategies to find the best BIST system



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Atrenta is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools and methodologies to capture design intent, explore implementation alternatives, validate RTL and optimize designs early, before expensive and time-consuming detailed implementation. With over 150 customers, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. **Atrenta, Right from the Start!**

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