



SpyGlass[®]-Power

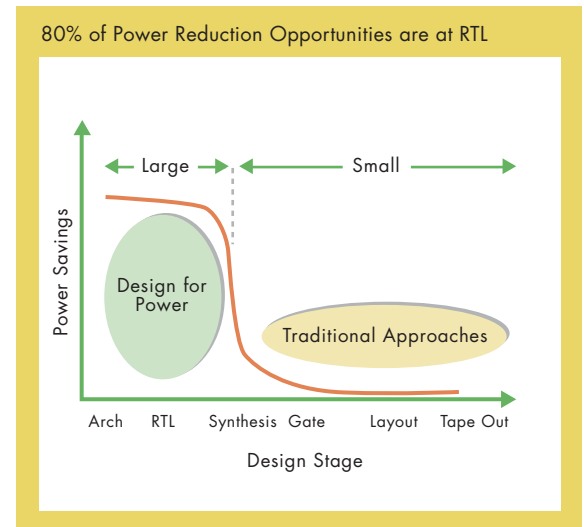
Design for Low Power from RTL



Previously, only IC designers of wireless applications need worry about power management. Today, tethered applications also need managed power for packaging and cooling costs. Beyond the fact that 80% of design-starts are constrained to under 2 watts, with each technology process, leakage power increases to rival dynamic power; at 90nm, it is nearly 40% of total power. Designers need to use every trick available to manage dynamic and leakage power – voltage domains, power domains, activity analysis, with power estimation, and start as early as possible – at RTL.

The Problem

- Each decrease in process geometry makes it harder to achieve leakage and dynamic power targets
- Designers at 90nm and below use multiple voltage domains and multiple power domains to manage power consumption
- The more active portions of the design use the most power. Even with simulation activity files, it is challenging to identify how to save power
- Domains which power-up/down out of sequence can cause functional failures
- After P&R and timing optimization, voltage domains and power domains may not be correctly connected and need to be independently verified
- Designers need an accurate “power number” for the chip as early in the RTL design process as possible

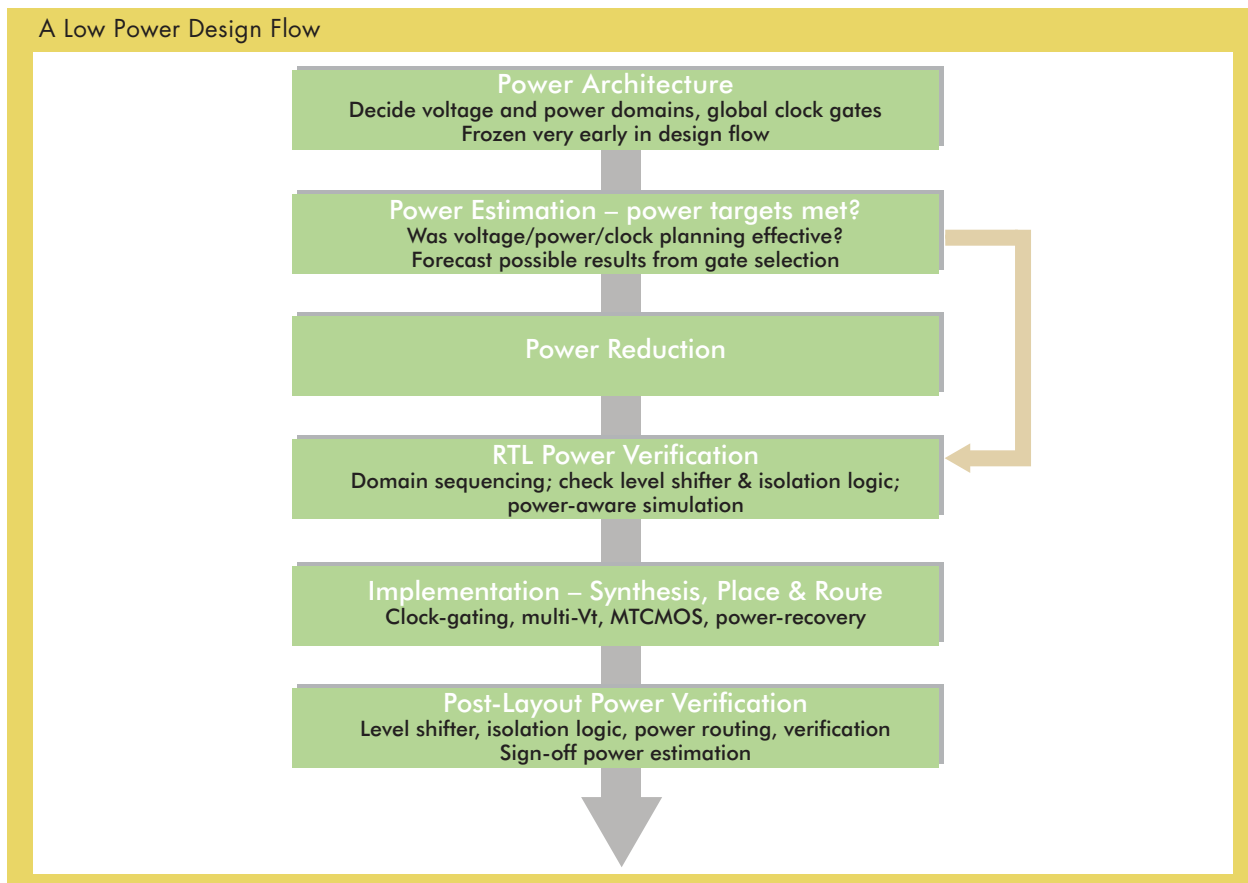


The Atrenta Solution – SpyGlass-Power

- Works from RTL, gates, or post-layout
- Checks correctness of voltage and power domains and automatically fixes errors
- Checks power/ground connectivity
- Measures clock gating effectiveness
- Finds additional clock gating opportunities and areas of high activity
- Ensures correct power domain sequencing
- Estimates power using simulation-based and vectorless power techniques
- Supports UPF and CPF power formats

SpyGlass-Power Methodology

- Provides a structured, easy to use and a comprehensive method for solving power design issues, thereby ensuring high quality RTL
- Provides methodology documentation and rule-sets as part of the product
- Walks users through a series of recommended steps to estimate power, reduce power, and ensure the design complies to 'power intent'



The Atrenta Difference

- Design for low power at RTL where impact is greatest
- Ensure at RTL that design meets power budget for package, cooling, battery life considerations
- Improve effectiveness of clock gating solution to reduce power
- Prevent silicon failure and respins due to:
 - > incorrectly inserted level shifters
 - > incorrectly inserted isolation logic
 - > incorrectly connected power/ground
 - > unexpected power-up/power-down behavior
- Integrates with Atrenta SpyGlass capabilities targeted for RTL like constraints, CDC and DFT



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Atrenta Inc. is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools & methodologies to optimize their designs early in the RTL phase for linting, clock domain crossings, power estimation and reduction, design for test, constraints generation and validation including timing exceptions, and RTL prototyping. **Atrenta, Right from the Start!**

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