

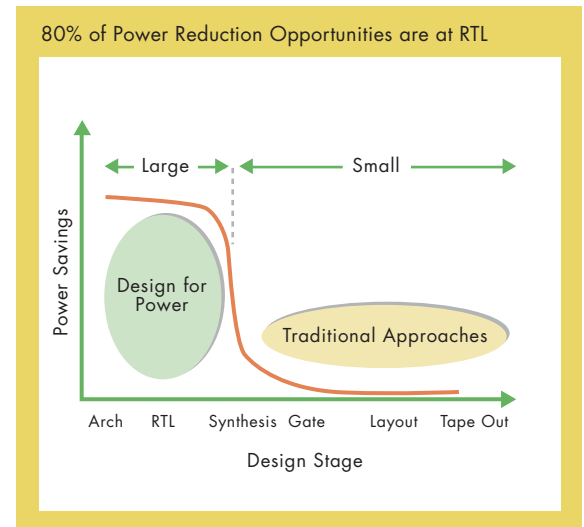
SpyGlass® Power

Design for Low Power from RTL

In the past, only IC designers of wireless applications worried about power management to extend battery life. Today, tethered applications also need to consume lower power to minimize packaging and cooling costs. Designers need to use every design trick available to manage dynamic and leakage power at deep submicron technologies and have to deal with multiple voltage domains and power domains. These involve performing activity analysis with different testbenches along with power estimations, and start as early as possible – at RTL.

The Problem

- Each decrease in process geometry makes it harder to achieve leakage and dynamic power targets
- Designers at 65nm and below use multiple voltage domains and multiple power domains to manage power consumption
- The more active portions of the design use the most power. Even with simulation activity files, it is challenging to identify how to save power
- Domains which power-up/down out of sequence can cause functional failures
- After P&R and timing optimization, voltage domains and power domains may not be correctly connected and need to be independently verified
- Designers need an accurate “power number” for the chip as early in the RTL design process as possible



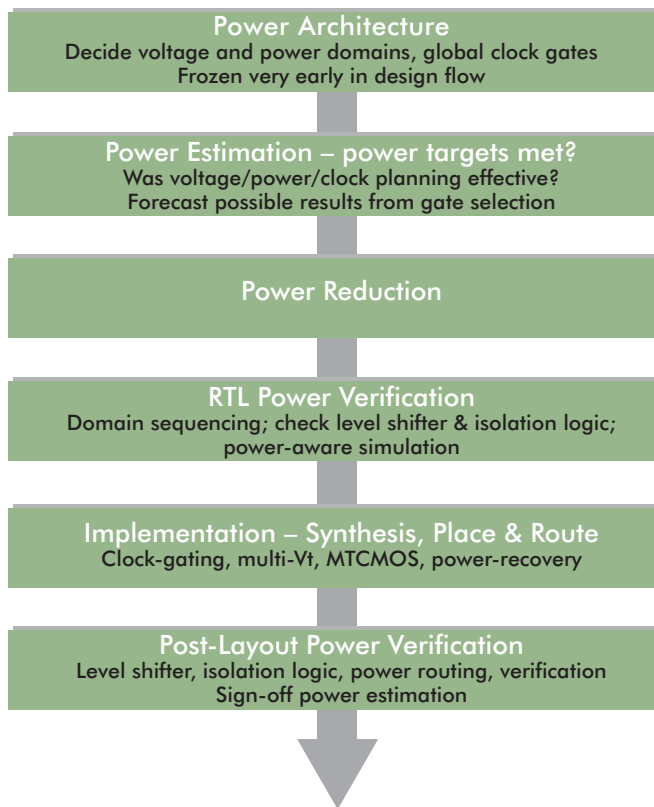
The Atrenta Solution – SpyGlass® Power

- Works from RTL, gates, or post-layout
- Supports UPF and CPF power formats
- Estimates power using simulation-based and vectorless power techniques and areas of high activity
- Measures clock gating effectiveness
- Helps reducing power at RTL by finding additional clock gating opportunities
- Generates new RTL with lower power
- Sequential equivalence checking helps validate that the functionality of the power reduced RTL is same as the original RTL
- Checks correctness of voltage and power domains
- Checks power/ground connectivity on post layout netlist

SpyGlass Power Methodology

- Provides a structured, easy to use and a comprehensive method for solving power design issues, thereby ensuring high quality RTL
- Provides methodology guidance and appropriate rule-sets for each stage of the design from RTL through synthesis to post place and route netlist
- Walks users through a series of recommended steps to estimate power, reduce power, and ensure the design complies to 'power intent' with either UPF or CPF formats

A Low Power Design Flow



The Atrenta Difference

- Design for low power at RTL where impact is greatest
- Ensure at RTL that design meets power budget for package, cooling, battery life considerations
- Improve effectiveness of clock gating solution to reduce power
- Prevent silicon failure and respins due to:
 - > incorrectly inserted level shifters
 - > incorrectly inserted isolation logic
 - > incorrectly connected power/ground
 - > unexpected power-up/power-down behavior
- Integrates with Atrenta SpyGlass capabilities targeted for RTL like lint, constraints, CDC & DFT



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Atrenta is a leading provider of SoC Realization solutions for the semiconductor and electronic systems industries. As one of the largest private electronic design automation companies, Atrenta provides a comprehensive SoC Realization solution that delivers higher quality semiconductor IP, predictable design coherence, automated chip assembly and improved implementation readiness. With over 170 customers, including 19 of the top 20 semiconductor and consumer electronics companies, Atrenta enables the most complex SoC designs in the world. Atrenta, the SoC Realization Company.

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