



GenSys™ Assembly

Architecture Generation & Programmed Handoff

The need for higher design efficiencies in all semiconductor product development has led to an increased focus on IP reuse and platform-based design techniques. The ability to perform comprehensive architectural planning/optimization and communicate the goals of the design to downstream team members with clear specifications and no ambiguity represent substantial competitive differentiation. The goal of these activities is always the same – leverage a design investment across multiple similar socket opportunities, and win those sockets through cost and time-to-market advantages. The GenSys™ Assembly product provides an environment to realize these goals.

The Problem

- Competitive pressures and short time-in-market drive a need to deliver multiple variants of a design very quickly, at low effective NRE per design
- There is a growing recognition that the complexity of chip logic assembly has become a major source of program delays and failures, yet in an era of high automation for RTL design it is still one of the least standardized phases in the design flow
- As design teams become geographically dispersed, consistency and correctness of design implementation data becomes a key challenge for chip integration teams
- Some tools have emerged over the past few years to address these problems, primarily focusing on modeling and verification. Support for production chip assembly, with the ability to provide an unambiguous programmed handoff to implementation teams has been ignored

The Atrenta Solution – GenSys Assembly

The GenSys Assembly solution has been developed over more than three years with a leading semiconductor company servicing consumer markets. The goal of this work has been to reduce front-end development effort for SoC platforms and derivative designs by more than an order of magnitude, while also dramatically reducing the level of human error in assembly. To accomplish these goals, Atrenta has developed a product that moves beyond early market concepts of platform-based design as the starting point for a new chip RTL, to a system which fully supports architectural planning and a programmed handoff to back-end design.

The GenSys Assembly solution provides a comprehensive environment that supports all aspects of IP import, architectural planning, generation, optimization and programmed handoff. The solution has been designed to reduce manual connectivity to the greatest degree possible and to simplify completing what remains. It combines register management under the same framework as design entry, allowing joint development and cross-checking of these views for concurrent development. At the end of the process, a programmed handoff to implementation is produced, which includes the automated production of a top-level netlist and timing/layout/test constraints.

GenSys Assembly Features

- Interface-based connectivity reduces user-defined connections by 95% or more. Ad-hoc connectivity is also supported through a high-productivity interface
- Support for a bottom-up design methodology through standard hierarchical methods, and a top-down design methodology through the ability to change hierarchy on the fly, and create/edit new components in place
- Support of a comprehensive set of connection techniques with splices and overrides to handle permanent and temporary tie-offs and opens – handling all the special cases that happen in real designs
- User-definable auto-connect techniques aid completion of many connections
- Comprehensive connectivity checking with sort/filter options to review how and why connections are made, and a direct connection to the SpyGlass® suite for a broad range of design analysis
- Traceability of who created an object or made a change and when
- Support for a spreadsheet-based paradigm, familiar to most designers with batch and graphical use-models, which are fully interchangeable
- Fully interoperable (import and export) with several standards including IP-XACT 1.2, Verilog and VHDL (both designs and components), CSV and Tcl
- Support for register management and automated netlist generation
- Support for template-based report generation, providing a simple way to generate custom reports
- Silicon proven on multiple designs

The Atrenta Difference

- Builds “correct-by-construction” chip and sub-system assemblies, reducing time to capture and debug
- Works smoothly even with a traditional RTL methodology
- Shows immediate benefits in turnaround-time for capture and edit of full-chip designs
- Reduces or eliminates the need for re-spins, potentially saving millions of dollars
- Enables early closure of hand-off ready chip netlists
- Helps dispersed design teams to create more consistent, high-quality designs
- Exploits the full power of effective design re-use and IP integration
- Integrates seamlessly into existing design environments, dramatically enhancing efficiency of installed tools and methodologies



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Atrenta is a leading provider of SoC Realization solutions for the semiconductor and electronic systems industries. As one of the largest private electronic design automation companies, Atrenta provides a comprehensive SoC Realization solution that delivers higher quality semiconductor IP, predictable design coherence, automated chip assembly and improved implementation readiness. With over 170 customers, including 19 of the top 20 semiconductor and consumer electronics companies, Atrenta enables the most complex SoC designs in the world. Atrenta, the SoC Realization Company.

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