

SpyGlass®

Early Design Analysis for Logic Designers

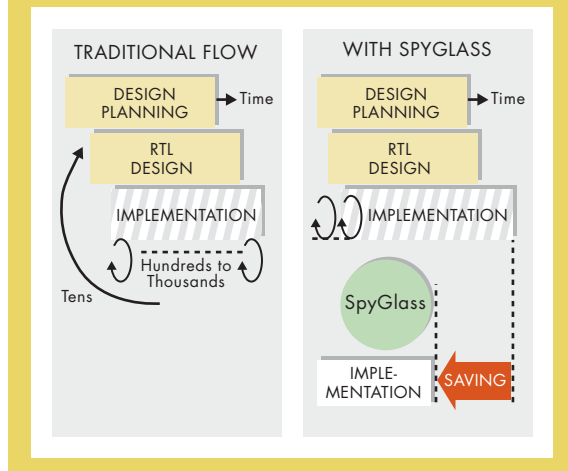


Inefficiencies during RTL design usually surface as critical design bugs during late stages of design implementation. If detected, these bugs will often lead to iterations, and if left undetected, will lead to silicon re-spin. The SpyGlass® product family is the industry standard for early design analysis with the most in-depth analysis at RTL design phase. The Spyglass solution provides an integrated platform for analysis, debug and fixing with a comprehensive set of capabilities for structural, functional, clocking and electrical issues all tied to the RTL description of design.

The Problem

- With soaring complexity and size of chips, achieving predictable design closure has become a challenge
- A multitude of design issues ranging from coding style, structural, functional, clocking and electrical can manifest themselves as design bugs and result in design iterations or worst still – silicon re-spins
- Other tools may detect design bugs but often at late stages of design implementation, after a significant investment in time and effort has already been made on the design
- As design teams become geographically dispersed, consistency and correctness of design intent becomes a key challenge for chip integration teams
- Emphasis on design re-use and IP integration requires that design elements being integrated meet guidelines for correctness and consistency

The SpyGlass Solution Accelerates and Economizes IC Development by Minimizing Costly, Time-consuming Design-and-debug Iterations.



The Atrenta Solution - SpyGlass

The SpyGlass solution greatly reduces the risk of developing complex multimillion-gate, nanometer-scale ICs by accurately detecting design issues at RTL. The SpyGlass solution flags areas of the design that are likely to present implementation challenges.

- Sophisticated static and dynamic analysis identifies critical design issues at RTL
- Industry-leading comprehensive clock, reset and clock domain crossing (CDC) analysis
- A comprehensive set of electrical rules checks to ensure netlist integrity
- Customizable framework to capture and automate company expertise
- Integrated debug environment enables easy cross-probing among violation reports, schematic and RTL source
- The most comprehensive knowledge base of design expertise and industry-standard best practices
- Supports Verilog, VHDL, V2K, SystemVerilog and mixed-language designs

ATRENTA®, **Right** from the Start!

SpyGlass Methodology

- Provides a structured, easy to use and comprehensive method for solving RTL design issues, thereby ensuring high quality RTL with fewer but meaningful violations
- Provides methodology documentation and rule-sets are provided as part of the product
- Provides an infrastructure for rule selection and customization aligned with design milestones
- Walks users through a series of recommended steps to ensure design compliance to HDL standards, coding style, synthesis, simulation, verification, connectivity finite-state machine, clock and reset issues
- This step-by-step approach detects and fixes design bugs in alignment with design milestones, and ensures predictable design closure without any last minute surprises or a high volume of violations

The Atrenta Difference

- Supports “correct-by-construction” design, leading to early design closure and minimizing costly back-end debugging and iterations
- Integrates with Atrenta SpyGlass capabilities targeted for RTL like constraints, power, CDC and DFT
 - > Easy to ramp up and begin productive use within half a day, even for non-experts.
 - > A structured methodology enables quick adoption by engineers and constraints optimized designs
- Reduces or eliminates need for re-spins, potentially saving millions of dollars
- Enables early closure of hand-off ready RTL design
- Elevates design optimization from gate-level to RTL, where it is most cost effective
- Helps dispersed design teams to create more consistent, high-quality designs
- Enables effective design re-use and IP integration
- Integrates seamlessly into existing design environments, dramatically enhancing efficiency of installed tools and methodologies



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Atrenta Inc. is the leading provider of Early Design Closure® solutions to radically improve design efficiency throughout the IC design flow. Customers benefit from Atrenta tools & methodologies to capture design intent, explore implementation alternatives, validate RTL and optimize designs early, before expensive and time consuming detailed implementation. With over 140 customers, including the world's top 10 semiconductor companies, Atrenta provides the most comprehensive solution in the industry for Early Design Closure. **Atrenta, Right from the Start!**

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